The Integrated Design Path of FPGA Reconfigurability and ASIC Specialization

Zhengxiong Su

New Epoch Bilingual School, Shanghai, China
zzzjkka@outlook.com

Abstract

This paper discusses the necessity, technical basis and implementation path of the integrated design of FPGA reconfigurability and ASIC specialization. The reconfigurability of FPGA enables it to flexibly adapt to different demands, while the specialization of ASIC brings about high performance and low power consumption. Converged design achieves a balance between performance, flexibility and cost through technological integration, architectural innovation and collaborative verification, and has broad application prospects in fields such as communication, AI and industrial control.

Keywords: FPGA reconfigurability; Specialization of ASIC; Integrated design; Technical path; Application scenarios

1. Introduction

In the field of integrated circuit design, FPGA (Field Programmable Gate Array) and ASIC (Application-Specific Integrated Circuit) have long been in a dynamic relationship of complementarity and competition [1]. FPGA, with its reconfigurability, demonstrates unique advantages in terms of hardware development cycle, cost adaptability and scenario flexibility [2]; Asics, through specialized design, dominate in terms of performance, power consumption and integration. With the acceleration of technological iteration, a single technical path has become difficult to meet the diverse demands of complex application scenarios [3]. The integrated design of FPGA and ASIC has become a key direction to break through technical bottlenecks.

The reconfigurability of FPGA stems from the flexible configuration capability of its internal logic units. By loading different configuration files, FPgas can repeatedly modify their internal circuit connections and functions on-site, achieving "hardware-level software-based adjustments" [4]. This feature gives it a significant advantage in scenarios where demands are rapidly iterated, such as communication protocol upgrades and AI algorithm optimizations, etc. For instance, the rapid evolution of 5G protocols from R15 to R18 demands that hardware be able to quickly adapt to the new standards. The flexibility of FPgas makes them the preferred choice for early verification and small-scale deployment [5]. However, the flexibility of FPgas comes at the expense of performance and power consumption: the universality of their logic units leads to increased signal transmission delay, and the power consumption is higher than that of specialized designs [6].

The specialization of ASics is achieved through full customization or semi-customization design, solidifying functions at the chip hardware level. Its advantages lie in high performance, low power consumption and high integration, but it lacks flexibility, has a long development cycle and is costly [7]. For instance, Apple's A-series chips achieve deep integration of CPU, GPU and NPU through specialized design, leading the performance of their contemporaries, but the development cost is as high as hundreds of millions of dollars [8]. In traditional design, FPGA and ASIC are often regarded as substitutive: FPGA is used for prototype verification and small-batch production, while ASIC is used for large-scale mass production. However, modern application scenarios have put forward higher requirements for hardware: on the one hand, the speed of demand iteration far exceeds the ASIC development cycle, such as the rapid evolution of 5G protocols from R15 to R18; On the other hand, single-function chips are difficult to meet the demands of multiple tasks. For instance, industrial controllers need to support motor drive, data acquisition and fault detection simultaneously [9]. Fusion design achieves a balance between performance, cost and development cycle by integrating the flexibility of FPGA with the efficiency of ASIC, and has become a core solution for addressing complex demands.

2. Technical Characteristics of FPGA and ASIC and the Necessity of Integrated Design

2.1 Comparison of Technical Features

The core feature of FPGA lies in the reconfigurability of its hardware logic. The logic units of FPGA (such as lookup Table LUT and digital signal Processing block DSP) are connected through an interconnection network, and users can define their functions and connection relationships through programming. This design enables it to dynamically adapt to different application scenarios, such as switching from communication baseband processing to image acceleration. High-end FPgas also integrate Hard IP cores, such as high-speed serial transceivers and PCIe controllers, further expanding their application scope. Asics achieve functional solidification through fully customized or semi-customized designs. Fully custom ASics are designed from the transistor level, optimizing the layout and routing of each logic unit to achieve the highest performance and the lowest power consumption. For instance, Google's TPU boosts AI inference throughput to 15 to 30 times that of a

GPU through dedicated matrix multiplication units. Semi-custom ASics (such as standard cell library designs) implement functions through the combination of predefined logic units (such as AND gates, OR gates), with a shorter development cycle than fully custom designs, but the space for performance and power consumption optimization is limited. The specialization of ASics makes them dominant in performance-sensitive scenarios such as high-performance computing and AI training, but they lack flexibility and are difficult to adapt to scenarios with rapidly changing demands.

2.2 The Necessity of Integrated Design

In traditional design, the substitution relationship between FPGA and ASIC has become difficult to meet the demands of modern applications. Take the field of communication as an example. The evolution of 5G protocols from R15 to R18 requires hardware to be able to quickly adapt to the new standards. If ASIC design is adopted, each protocol upgrade requires re-tape-out, with a development cycle of up to 18 to 24 months and costs as high as tens of millions of dollars. Although FPgas can rapidly reconfigure logic, their performance and power consumption are difficult to meet the requirements of large-scale deployment: for instance, the processing latency of 5G basebands implemented by FPgas is 30% to 50% higher than that of ASics, and the power consumption increases by 2 to 3 times. The fusion design achieves a balance between performance and flexibility by embedding ASIC hard cores (such as 56G SERDES) in the FPGA: the hard core handles high-speed signal transmission, and the programmable logic enables dynamic updates of protocol logic, allowing the hardware to simultaneously meet the requirements of high performance and rapid iteration.

Multitasking requirements are another driving factor for converged design. For instance, industrial controllers need to support motor drive, data acquisition and fault detection simultaneously. Traditional designs require multiple dedicated chips, which are costly and take up a lot of space. Although FPgas can achieve multi-task support through logic reconfiguration, their long-term operational stability is insufficient: for instance, FPgas are prone to configuration bit flipping in high-temperature environments, leading to functional abnormalities. The fusion design integrates FPGA programmable resources through ASIC to achieve multi-task support: ASIC hardcore processes high-speed control logic (such as PWM signal generation), and programmable logic implements low-speed auxiliary functions (such as temperature monitoring), which not only ensures the performance of critical tasks but also reduces overall power consumption. In addition, the integrated design supports long life cycle maintenance. For instance, after the launch of space exploration equipment, it cannot be physically repaired. Hardware vulnerabilities or new functions (such as the extended image processing capabilities of NASA's Mars probe) can be fixed through FPGA reconstruction, thereby extending the service life of the equipment.

3. The Technical Foundation of Integrated Design

3.1 Hardware Architecture Innovation

High-end FPgas expand their application range by integrating ASIC Hard IP cores. For example, Altera's Stratix V GX devices are embedded with 28G SERDES hard cores, Xilinx's Virtex6 series supports PCIe 3.0 protocol hard cores, and Lattice's SC series FPgas integrate SONET/SDH standard application units. This type of design combines the high-speed and low-power consumption characteristics of ASics with the flexibility of FPgas, significantly reducing the design difficulty and shortening the development cycle. Take the communication field as an example. The 56G SERDES hard core embedded in the FPGA can directly support the baseband processing of 5G base stations without the need for additional ASIC development.

ASIC achieves Structured ASIC design by integrating programmable logic units (such as the LUT and DSP Block of FPGA). For instance, some ASics reserve programmable areas within the chip and achieve functional customization through metallization processes. This not only retains the performance advantages of ASics but also enables local reconfiguration capabilities. This design is widely applied in the field of automotive electronics. For instance, the engine control unit can adapt to the requirements of different vehicle models by reconfiguring some of its logic, thereby reducing the types of dedicated chips.

3.2 Optimization of Interconnection Technology

The integration of FPGA and ASIC puts forward higher requirements for the interconnection network: it is necessary to achieve low-latency and high-bandwidth data transmission under the premise of ensuring signal integrity. Modern FPgas adopt a hierarchical interconnection structure, optimizing signal transmission at different distances through the combination of Length1, Length4 and the dedicated interconnection line Length2. For instance, Altera's Fastrack technology enables full-device data transmission through horizontal/vertical axis interconnection paths, while Xilinx's dynamic reconfigurable architecture supports SIMD (Single Instruction Multiple Data) and Systolic computing modes, enhancing parallel processing efficiency.

3.3 Collaborative Verification Method

The integration design needs to address the compatibility issues between the FPGA and ASIC design processes. Traditional ASIC design relies on RTL (Register Transfer Level) code synthesis and physical implementation, while FPGA design directly generates configuration files through HDL (Hardware Description Language). Collaborative verification achieves the mapping between functional description and physical implementation through a unified design language and simulation tools. For instance, advanced HDL languages such as SystemVerilog and SystemC support system-level description and can be used simultaneously for FPGA prototype verification and ASIC comprehensive optimization. EDA tools such as Vivado

and Quartus offer FPGA-to-ASIC conversion capabilities, automatically generating gate-level netlists and layout and routing files.

4. The Implementation Path of Integrated Design

4.1 Technology Integration

The core of technological integration is to break the physical boundaries between FPGA and ASIC, achieving mutual embedding of resources and symbiotic functions. Early fusion was mainly based on functional embedding, such as integrating ASIC hard cores in FPgas or vice versa. With the development of technology, architectural symbiosis has become mainstream. For instance, Microsoft's Catapult project integrates FPgas on a large scale into Azure data centers and achieves dynamic allocation of hardware resources through a Shell-Role separation architecture: The Shell layer solidifies the underlying functions (such as PCIe interfaces and DDR4 controllers), while the Role layer loads application logic (such as DNN inference accelerators). All FPgas are interconnected through a dedicated high-speed network to form a decentralized acceleration cluster. This type of design enables FPgas to maintain flexibility while approaching the throughput capacity of ASics.

4.2 Architectural Innovation: Dynamic Refactoring and Heterogeneous Integration

Architectural innovation focuses on enhancing the efficiency and adaptability of integrated design. Dynamic reconfiguration technology achieves real-time switching of hardware functions through partial reconfiguration. For instance, FPgas can serve as AI inference accelerators in data centers during the day and be restructured into radar signal simulators at night, making full use of hardware resources. Heterogeneous integration builds a unified computing platform by integrating heterogeneous computing units such as CPU, GPU, and DSP. For example, Xilinx's Zynq series SoC integrates ARM Cortex-A series processors and FPGA logic, supports software and hardware co-design, and is suitable for complex scenarios such as autonomous driving and industrial Internet of Things.

4.3 Collaborative Verification

Collaborative verification runs through the entire process of integrated design, covering functional verification, performance optimization and reliability testing. Functional verification verifies the logical correctness of the ASIC design through FPGA prototypes to avoid the risk of tape-out failure. For instance, chip design companies often use FPgas to build CPU prototypes and verify instruction sets and caching mechanisms. AI algorithm developers test the hardware acceleration effect in real time through FPgas and optimize the neural network structure. Performance optimization is achieved through system-level simulation tools such as VCS and ModelSim to analyze timing, power consumption, and area (PPA) metrics, guiding design iterations. Reliability testing focuses on the specific challenges of fusion design, such as signal integrity during the FPGA reconfiguration process and the interoperability stability between ASIC hard core and programmable logic.

5. Application Scenarios of Integrated Design

5.1 Communication Field: Rapid Protocol Iteration and Multi-standard Support

The rapid iteration of communication protocols is a typical application scenario of converged design. For instance, 5G base station chips need to support protocol evolution from R15 to R18. Traditional ASIC design requires multiple tape-out processes, which is costly. FPGA can adapt to new protocols by reconfiguring logic, but its performance is limited. The fusion design achieves a balance between performance and flexibility by embedding ASIC hard cores (such as 56G SERDES) in the FPGA: the hard core handles high-speed signal transmission, and the programmable logic realizes dynamic updates of protocol logic. Furthermore, the integrated design supports multi-standard compatibility. For instance, the same base station chip can simultaneously support 4G LTE and 5G NR protocols, reducing the deployment costs for operators.

5.2 AI Field: Algorithm Iteration and Adaptation to Edge Computing

The rapid iteration of AI algorithms poses severe challenges to hardware. For instance, since the Transformer model was proposed in 2017, it has given rise to dozens of variants such as MoE and ViT, making it difficult for fixed-architecture chips (like TPU) to be compatible. Although FPgas are reconfigurable, their inference latency and energy efficiency ratio are lower than those of ASics. Fusion design achieves dynamic adaptation of algorithms to hardware through a software and hardware collaborative compilation stack (such as the Microsoft Brainwave project) The compiler automatically maps the ONNX model to the FPGA pipeline. The on-chip SRAM optimizes the weight cache and dynamically batch adjusts the input size, enabling the FPGA to achieve inference performance close to that of the ASIC while maintaining flexibility (e.g., ResNet-50 latency <1ms, throughput >390,000 images/sec). In edge computing scenarios, fusion design enhances hardware utilization and reduces equipment costs by allocating resources on demand (such as processing video streams during the day and analyzing sensor data at night).

5.3 Industrial Control: Multi-task Support and Long Lifecycle Maintenance

Industrial control scenarios are extremely sensitive to the reliability, flexibility and cost of hardware. For instance, if the same device needs to support motor drive, data acquisition and fault detection simultaneously, the traditional design requires multiple dedicated chips, which is costly. Although FPgas are reconfigurable, their long-term operational stability is insufficient. The fusion design integrates FPGA programmable resources through ASIC to achieve multi-task support: ASIC

hardcore processes high-speed control logic (such as PWM signal generation), and programmable logic implements low-speed auxiliary functions (such as temperature monitoring), which not only ensures the performance of critical tasks but also reduces overall power consumption. In addition, the integrated design supports long life cycle maintenance. For instance, after the launch of space exploration equipment, it cannot be physically repaired. Hardware vulnerabilities or new functions (such as the extended image processing capabilities of NASA's Mars probe) can be fixed through FPGA reconstruction, thereby extending the service life of the equipment.

5.4 Aerospace: High Reliability and Dynamic Mission Adaptation

The aerospace field has extremely high requirements for the reliability, radiation resistance and dynamic mission adaptability of hardware. For instance, satellites need to operate in orbit for 5 to 10 years, during which they must be adapted to various tasks (such as air exploration and sea search). Traditional ASIC design requires the development of dedicated chips for each task, which is unaffordable in terms of cost. Although FPgas are reconfigurable, their radiation resistance is insufficient. The fusion design achieves high reliability by integrating FPGA anti-radiation units (such as three-mode redundant SRAM) into the ASIC: the ASIC hardcore processes core computing tasks (such as navigation algorithms), programmable logic realizes dynamic task switching, and at the same time, the anti-radiation performance is enhanced through redundant design. For instance, after a certain type of satellite adopted the fusion design, the mission adaptation time was shortened from several months to just a few hours, and the hardware failure rate was reduced by 80%.

6. Conclusion

The integrated design of FPGA reconfigurability and ASIC specialization is an inevitable trend in the development of integrated circuit technology. Through technology integration, architectural innovation and collaborative verification, integrated design breaks through the limitations of a single technology and achieves a dynamic balance among performance, flexibility and cost. In the future, with the maturation of advanced technologies such as 3D packaging and Chiplet, fusion design will further develop towards high integration, low power consumption and intelligence, becoming a key infrastructure in fields such as communication, AI, industrial control and aerospace.

References

[1] Ashakin, M. R., Hossain, B., & Ifty, S. M. H. (2024). Enhancing Digital Signal Processing: Obstacles and Advancements in FPGAand ASIC Hardware Implementations. Pathfinder of Research, 2(2), 25-36.

[2] Bobda, C., Mbongue, J. M., Chow, P., Ewais, M., Tarafdar, N., Vega, J. C., ... & Tessier, R. (2022). The future of FPGA acceleration in datacenters and the cloud. ACM Transactions on Reconfigurable Technology and Systems (TRETS), 15(3), 1-42.

[3] Kang, B. J., Lee, H. I., Yoon, S. K., Kim, Y. C., Jeong, S. B., & Kim, H. (2024). A survey of FPGA and ASIC designs for transformer inference acceleration and optimization. Journal of Systems Architecture, 155, 103247.

[4] Lou, H. (2025, February). Comparative Analysis and Enhancement. In Proceedings of the Second International Conference on Artificial Intelligence and Communication Technologies (ICAICT 2024): Network Technologies, AI and DL, Volume 2 (Vol. 425, p. 295). Springer Nature.

[5] Abdulsamad, A. A., & Répás, S. R. (2025). Application of FPGA devices in network security: A survey. Electronics, 14(19), 3894.

[6] Sato, T., Chivapreecha, S., Moungnoul, P., & Higuchi, K. (2016, October). An FPGA architecture for ASIC-FPGA Co-design to streamline processing of IDSs. In 2016 International Conference on Collaboration Technologies and Systems (CTS) (pp. 412-417). IEEE.

[7] Sigala, N. S. (2025). Edge AI for Energy-Efficient Computing: A Systematic Review of Strategies, Challenges, and Future Directions. International Journal of Business & Computational Science, 2(1).

[8] Yevgeni, Y. (2024). IMPLEMENTATION OF ARTIFICIAL INTELLIGENCE ALGORITHMS IN FPGA/ASIC HARDWARE PLATFORMS. Universum: технические науки, 11(11 (128)), 5-10.

[9] Lin, T. J., Zhang, W., & Jha, N. K. (2014). A fine-grain dynamically reconfigurable architecture aimed at reducing the FPGA-ASIC gaps. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 22(12), 2607-2620